

AC/DC: Automated Compilation for Dynamic Circuits

Ed Younis







BQSKit's Amazing Multi-Institutional Team



Costin lancu



Ed Younis



Bert de Jong



Efekan Kökcü Mathias Weiden

Justin Kalloor









F • •

Past Members:

- Xin-Chuan Wu (Intel)
- Ethan Smith (NVIDIA)
- Tirthak Patel (Rice)
- Lindsay Bassman (CNR Nano)

BOSKit

2

Aaron Szasz (Google)

Siyuan Niu

Anupam Mitra

Ji Liu

Roel van Beeumen Marc Davis

Berkeley Quantum Synthesis Toolkit (BQSKit)

Powerful and portable quantum compiler framework built on numerical instantiation

Berkeley Quantum Synthesis Toolkit (BQSKit) [bis • kit]

Powerful and Portable Quantum Compiler Framework

- Gracefully handles every gate set and architecture
- Specialized pipelines for widely-used chips
- Generates resource efficient circuits (width, depth, timing, etc)
- Error mitigation
- Enables effective algorithm and hardware design exploration
- 20+ papers (3 IEEE QCE best papers: 2020, 2021, 2022)
- 500K+ downloads

Users:

- I ANI
- Sandia
- ANL
- ORNL
- LLNL
- U Penn
- U Del •

- U Chicago
- U Kansas ٠
- U Tokyo ٠

U Wisc

- NCSU ٠
- Duke •

٠

- CUNY

- Quantinuum
- Inflegion •
- AWS
- Microsoft
- NVIDIA
- UnitaryFund •
- HSBC



bqskit.lbl.gov

Turn-key Functionality that Works Everywhere

pip install bqskit

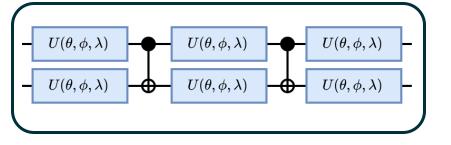
Python 3.8+ on Windows, Mac, Linux (from laptop to supercomputer)

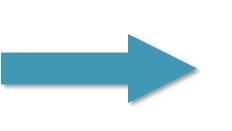
import bqskit out_circuit = bqskit.compile(circuit)

Any gate set or architecture in or out qubits, qudits, states, many-states, unitaries, and more (from experiment to real hardware)

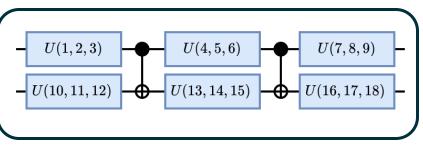
Parameterized Circuit Instantiation: A Powerful Primitive

Parameterized Circuit





Instantiated Circuit



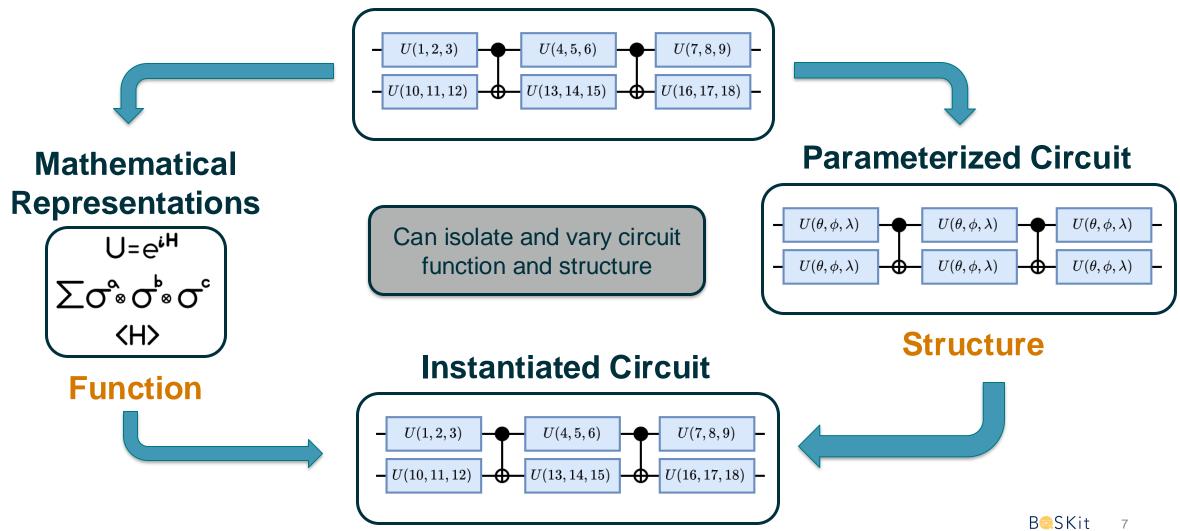
Parameterized Circuit Instantiation

Given a parameterized quantum circuit $C : \mathbb{R}^k \mapsto U(N)$ and a target unitary $V \in U(N)$, solve for $\underset{\alpha}{\operatorname{argmax}} tr(V^{\dagger}C(\alpha))$

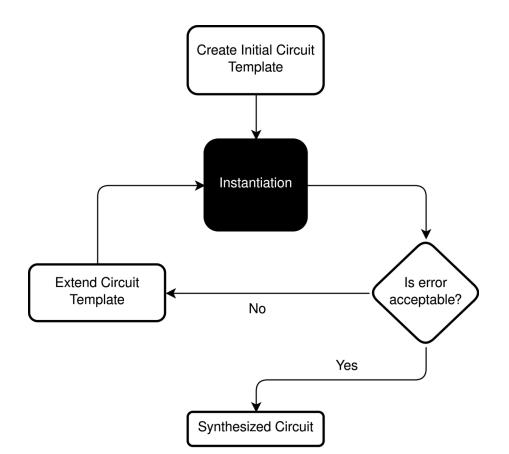


Instantiation Enables Function and Structure Separation

Instantiated Circuit

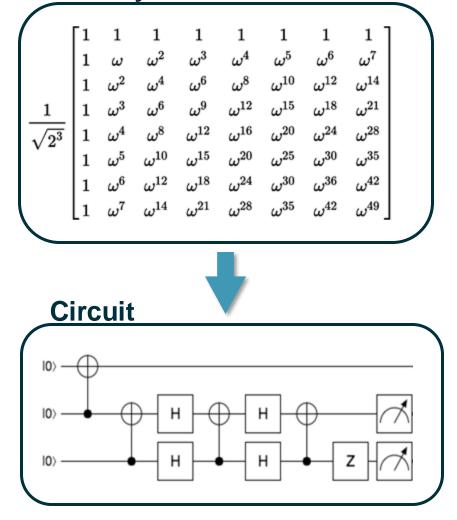


Instantiation is the Core of Bottom-Up Synthesis



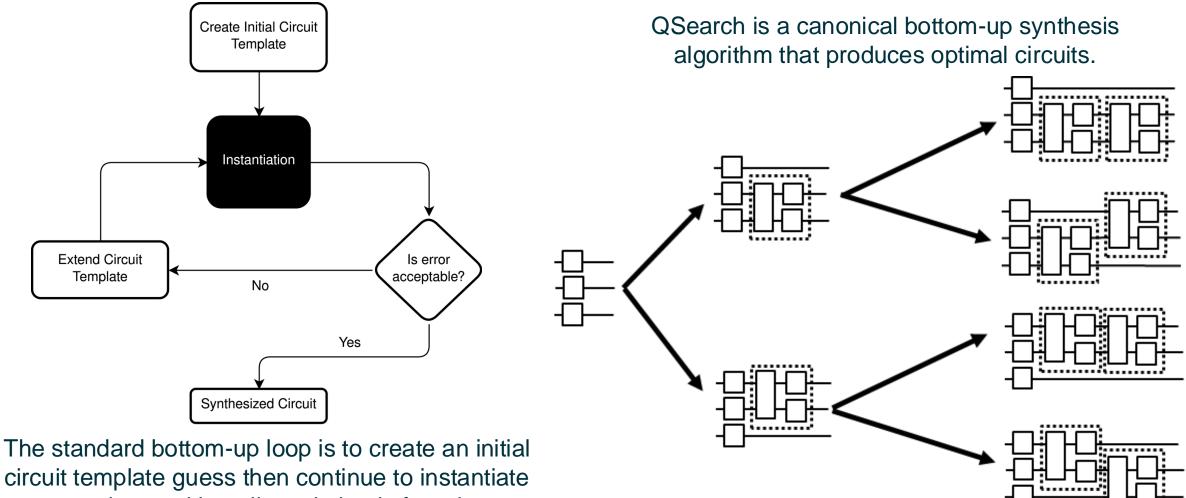
The standard bottom-up loop is to create an initial circuit template guess then continue to instantiate and extend it until a solution is found

Unitary



E. Younis et al., "QFast: Conflating Search and Numerical Optimization for Scalable Quantum Circuit Synthesis." 2021 IEEE International Conference on Quantum Computing and Engineering (QCE). IEEE, 2021. (Best Paper Award)

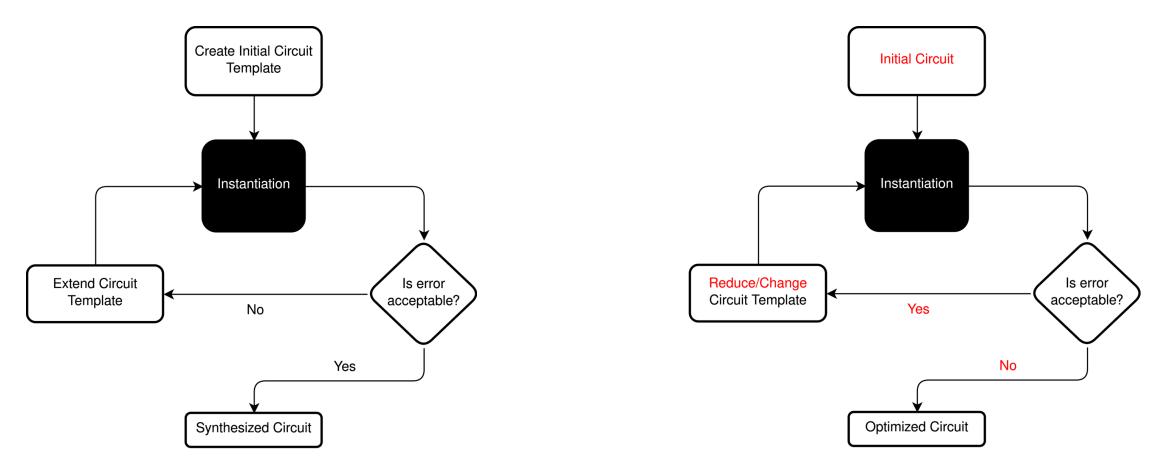
Instantiation is the Core of Bottom-Up Synthesis



and extend it until a solution is found

M. Davis et al., "Towards Optimal Topology Aware Quantum Circuit Synthesis." 2020 *IEEE International Conference on Quantum Computing and Engineering (QCE)*. IEEE, 2020. (Best Paper Award)

Instantiation-Based Circuit Transformation Flow



We have found Instantiation can also be used to transform or optimize a quantum circuit. Instead of extending a circuit template like in bottom-up synthesis, we reduce or transform a circuit template and continue until it is no longer successful or necessary.

Gate Deletion is Straight Forward with Instantiation

1) Remove a gate 3b) Reject new circuit if 2) Instantiate • error is unacceptable

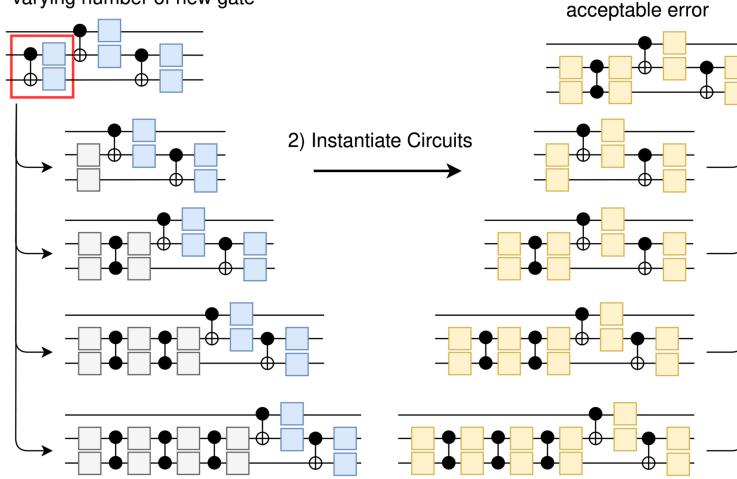
3a) Accept new circuit if error is acceptable

- Suboptimal circuits can have gates removed and others reinstantiated to accommodate the loss
- Gate deletion + Candidate selection = Optimization algorithm
- Extremely portable and flexible
- Very effective due to global transformations

Instantiation can Retarget Circuits without Rules

3) Select best circuit with

1) Replace gate wtih varying number of new gate



- Typically gate rebasing is done with fixed rules or analytic instantiation (KAK) that only consider local circuit changes
- Numerical instantiationbased rebasing is more effective, portable and flexible
- Works with gate sets contain multiple entangling gates

Instantiation-Based Algorithms in BQSKit

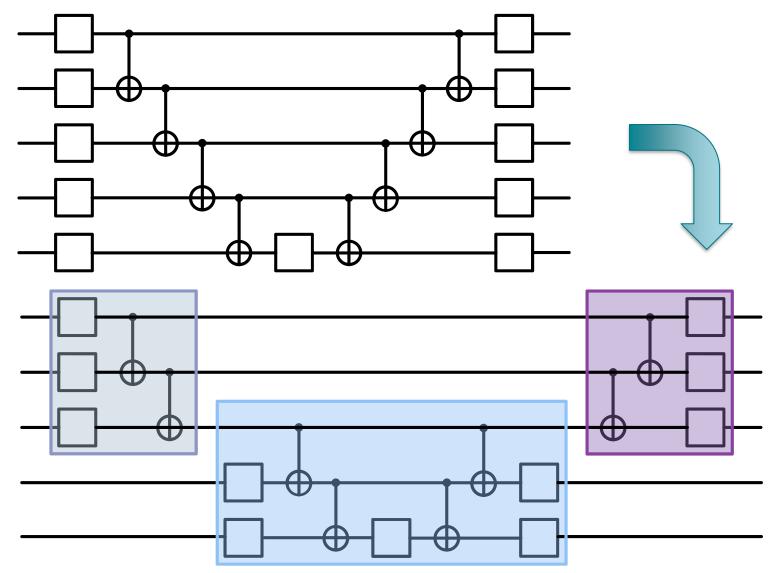
- QSweep 1 qudit, pulse-optimal
- QSearch 2-4 qudits, optimal
- PAS 3-4 qudits, better-than-optimal + post-processing
- LEAP 4-6 qudits
- QFAST 5-8 qudits
- QPredict 6-12 qudits



- Retargeting
- Gate Deletion
- Template Substitution
 - Circuit Resizing

Circuit Transformation

Partitioning Scales Instantiation to 1000s of qubits

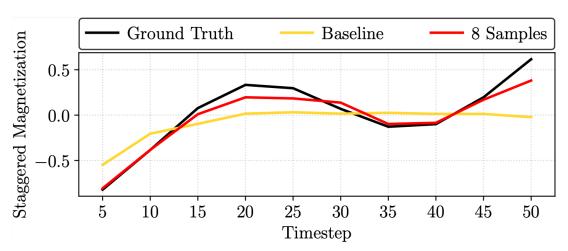


- Circuit on the left is partitioned into 3-qubit blocks below
- Partitioning overcomes the exponential scaling of numerical instantiation
- Restricts global view; can adjust block size for better performance or quality
- Creates an extremely parallel workflow

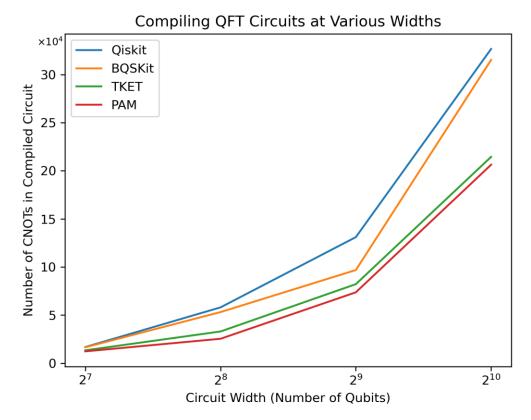
Instantiation-Based Workflows in BQSKit

Workflows

- Optimization (QGO, TopAS, Gate Deletion)
- Mapping/Routing (Generalized SABRE, PAM)
- Approximations (QuEST)
- Gate Set Retargeting
- Circuit Resizing

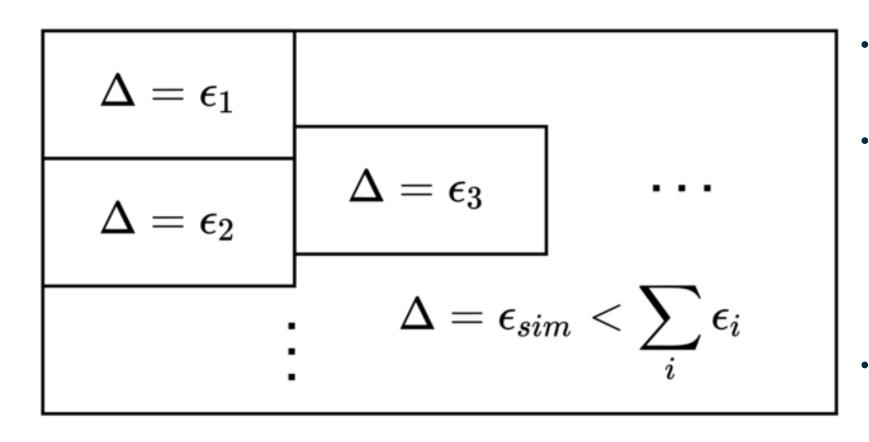


Approximations workflows better track ground truth on NISQ devices



PAM maps circuits with fewer final gates than commercial compilers

Push-button Compiler Verification



- Small circuits can have their error directly calculated
- Larger circuits can be first partitioned into large simulatable sections, then summing the section errors gives an upper bound on total error
- Unless specified, we target 10⁻⁸ to 10⁻¹⁰ instantiation verification error, most often it is less

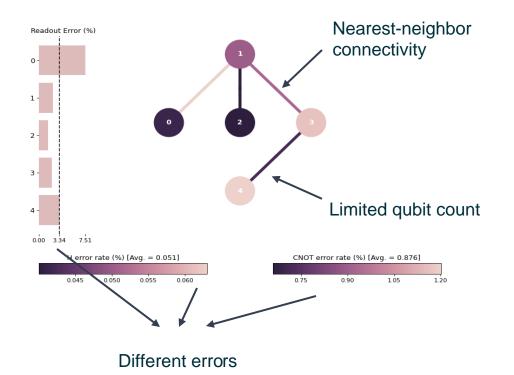
Effective Quantum Resource Optimization via Circuit Resizing in BQSKit

Discovering qubit reuse potential in previously impossible circuits via instantiation

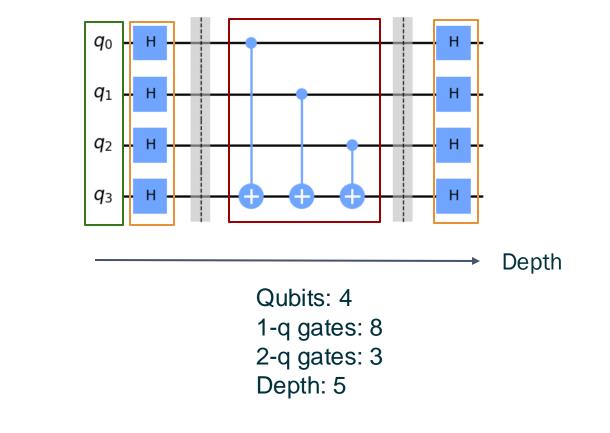
Niu, Siyuan, et al. Proceedings of the 61st ACM/IEEE Design Automation Conference. 2024.

Quantum Computing Requires Resource Optimization

Why do we need resource optimization?

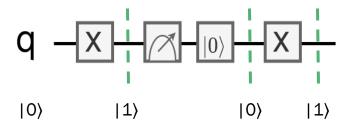


How to characterize resource?



Mid-circuit Measurement and Reset enables Resizing

• What is mid-circuit measurement and reset (MMR)?



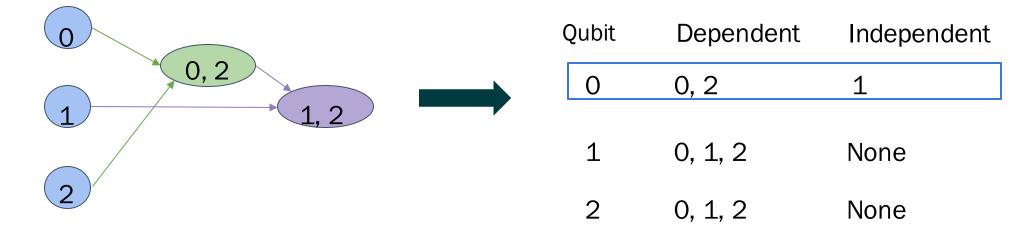
• How to use MMR for circuit resource optimization?



How to Realize Circuit Resizing?



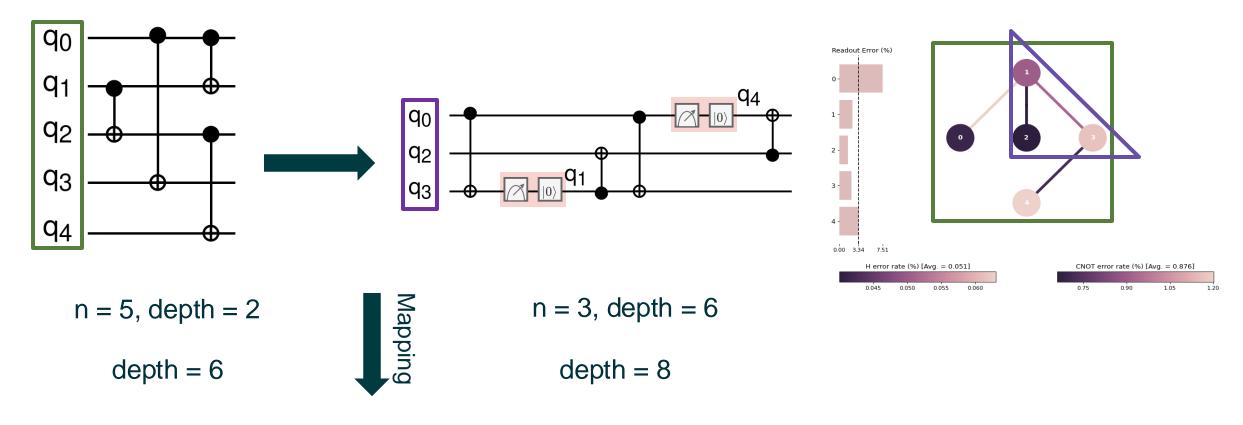
• By gate dependency graph!



• Not all the circuits are resizable by gate-dependency graph!

Gate-Dependency Based Resizing

- What can we get from circuit resizing?
 - o Use qubits with higher fidelity
 - Reduce the mapping overhead

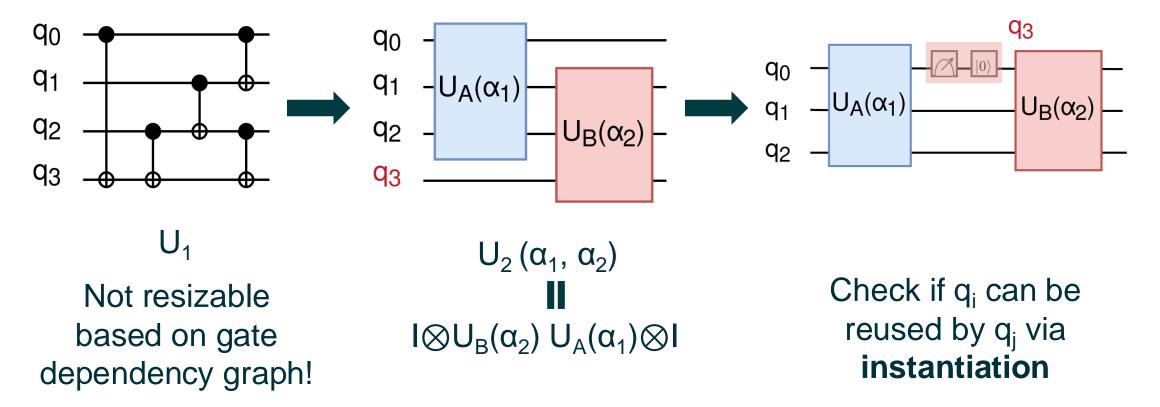


Resizable Checking via Instantiation

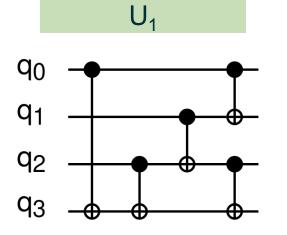
Can non-resizable circuit become resizable?

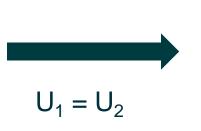
Resizable Checking via Instantiation

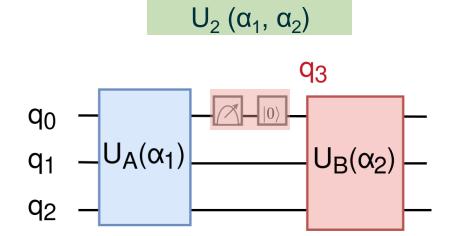
Can non-resizable circuit become resizable? - Yes, under constraints!



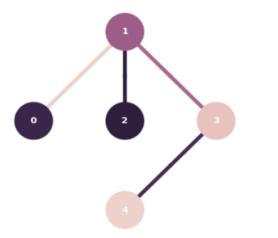
Instantiation-Based Resizing

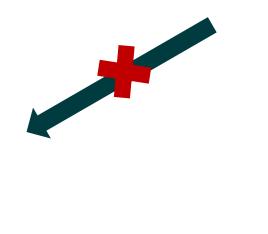




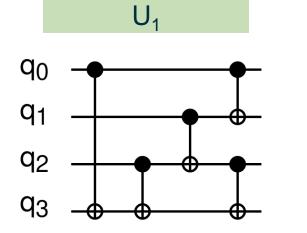


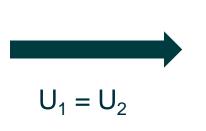
Only accepts two-qubit and single-qubit gates!



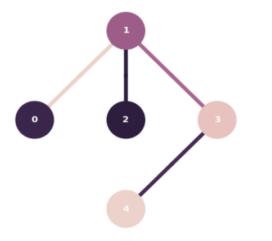


Instantiation-Based Resizing



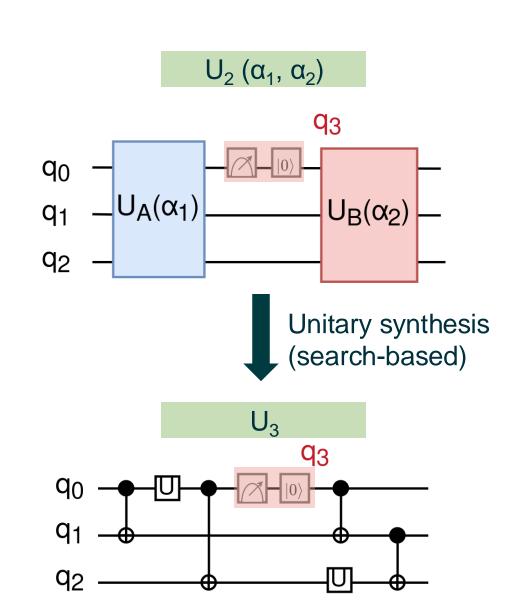


Only accepts two-qubit and single-qubit gates!



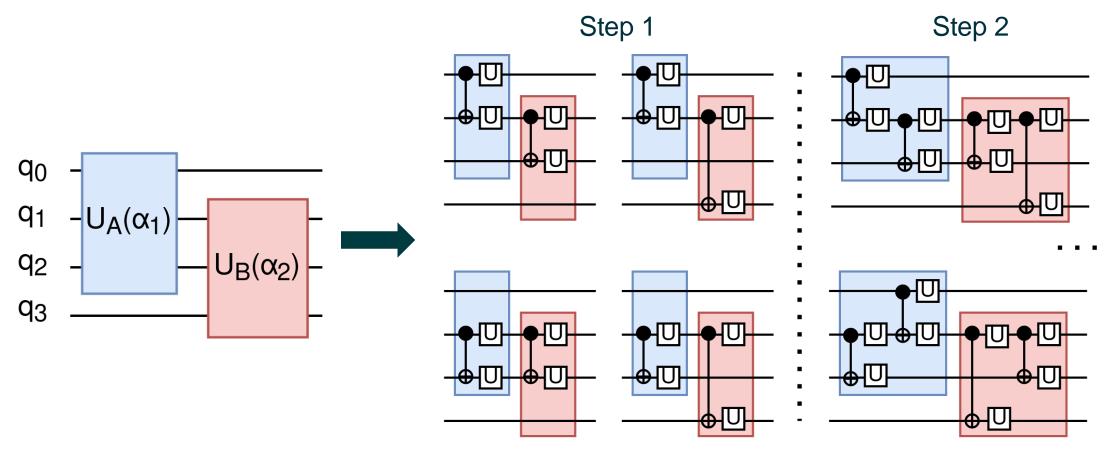
 $U_1 = U_2 = U_3$

Executable!



Two-block Simultaneous Unitary Synthesis

- Synthesize two n-1 blocks simultaneously with block structure constraints
- Topology aware (no need mapping or routing)



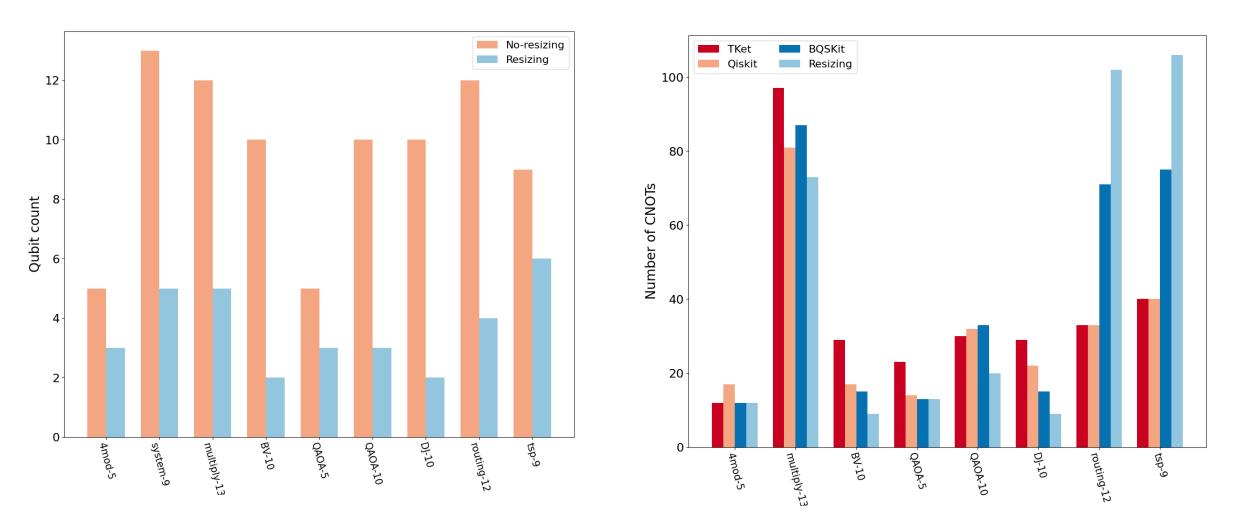
Experimental Setup

- Our resizing algorithms are built on top of BQSKit using Python 3.11.4.
- Comparison
 - Qiskit
 - Tket
 - BQSKit
- Benchmarks
 - VQE, QAOA, Bernstein-Vazirani, ...
- Evaluations on two IBM Quantum hardware
- Our code is available on Github! Try it out!



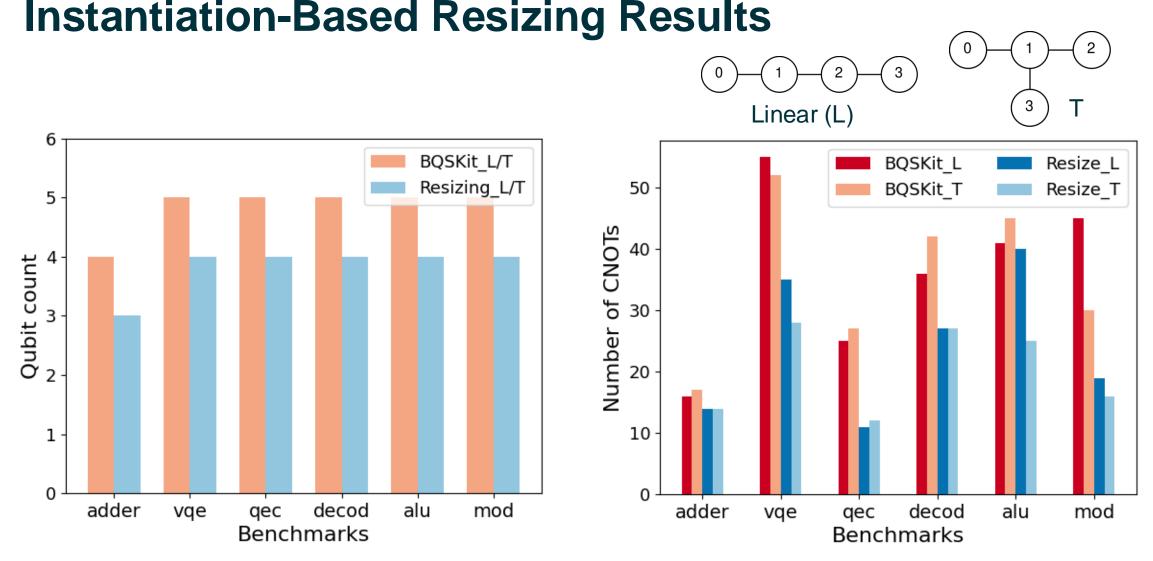
github.com/bqskit/bqskit-resize

Gate-Dependency Resizing Results



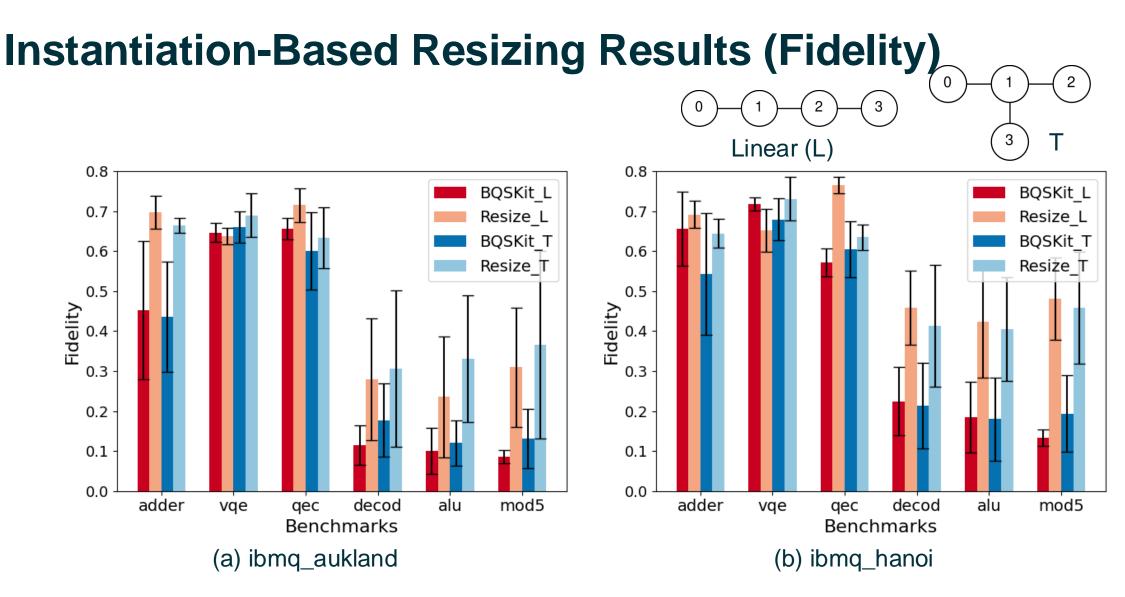
We reduce qubit count by 61.6% and #CNOT by 11.4%.

B@SKit 28



We reduce qubit count by 20.7% and #CNOT by 33% and 42.7% when compiled to linear (L) or T topology.

B@SKit 29



We improve circuit fidelity by **28.5%** and **28.4%** for two chips with linear topology, and by **28.9%** and **26.6%** with T topology.

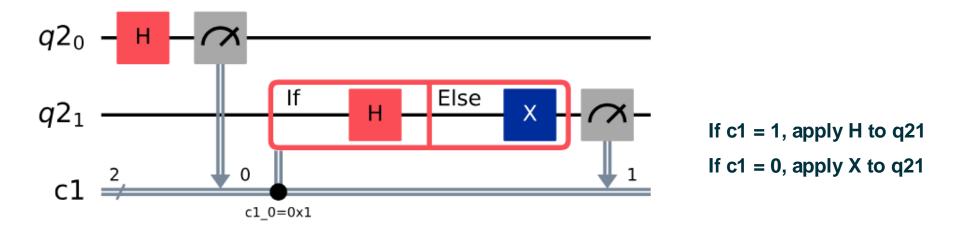
AC/DC: Automated Compilation for Dynamic Circuits

Empowering instantiation with dynamic circuit capabilities

Niu, Siyuan, et al. arXiv preprint arXiv:2412.07969 (2024).

Dynamic Circuits for Resource Optimization

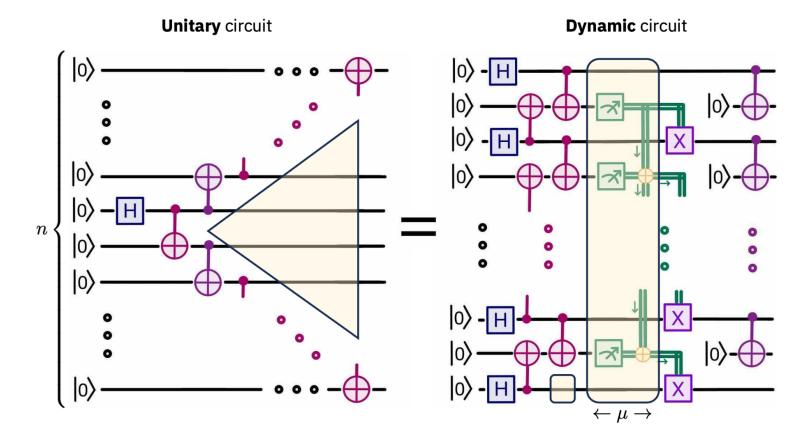
- Dynamic circuits include mid-circuit measurement and feed-forward.
- Measuring some qubits and applying feed-forward operations to the un-measured qubits.



• Quantum resource optimization: reduce circuit depth and #CNOTs

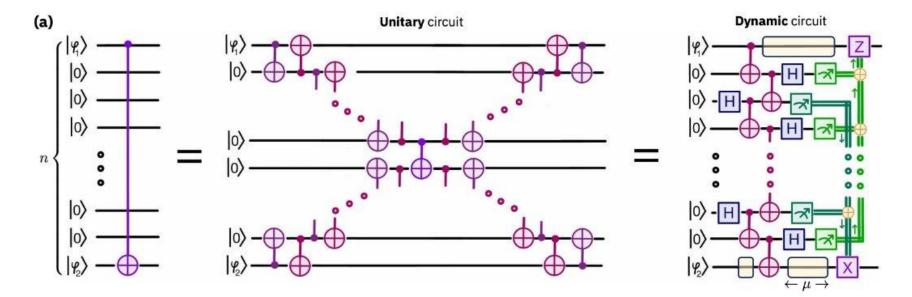
Constant-Depth GHZ State Preperation

• Achieving GHZ state preperation on linear topology with constant depth manually.



Optimizing long-range CNOT

• Achieving long range CNOT on linear topology with constant depth manually.



- Other applications in resource optimization
 - Quantum Fourier transformation
 - Quantum phase estimation
 - Quantum teleportation in circuit cutting

Optimizing long-range CNOT

Achieving long range CNOT on linear topology with constant depth manually.

(a) How to automatically generate dynamic circuits for arbitrary states or unitary operators? Other applicat

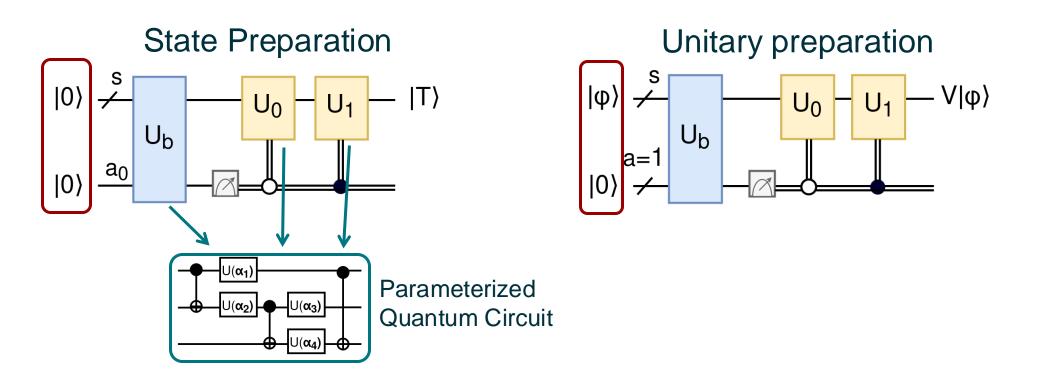
- Quantum Fou

n

- Quantum phase esumation
- Quantum teleportation in circuit cutting

Corcoles et al. PRL 2021, Baumer et al. PRL 2024, Baumer et al. PRX Quantum 2024, Nature 636, 75–79 (2024)

Automated Instantiation of Dynamic Circuits

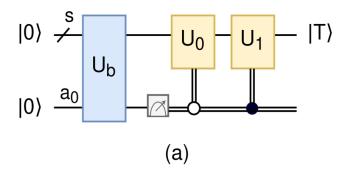


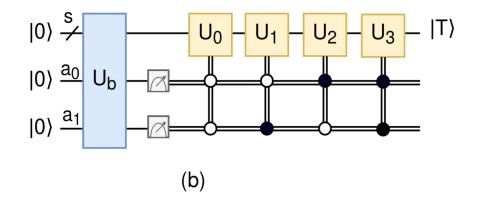
Goal: Find parameters in U_b and U_i to prepare the target state or unitary V. **Challenge**: How to deal with the non-unitary operations in synthesis?

Cost Functions for Dynamic State Preparation

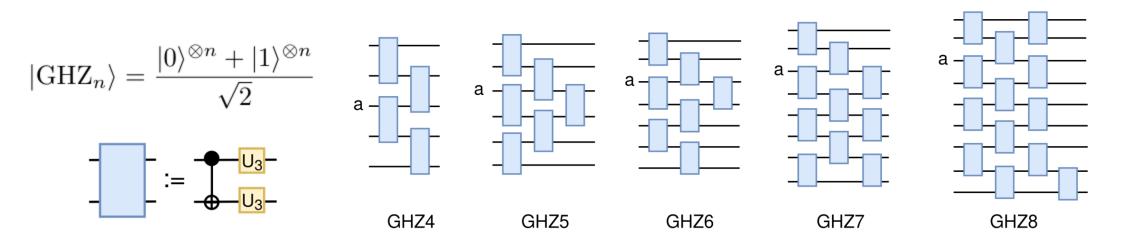
- Parameters
 - o s System qubits
 - o a Ancilla qubits
 - $_{\odot}$ U_{b} Unitary applied to all the qubits
 - \circ U_i Conditional unitary applied to system qubits
 - T Target state
- Cost Function (C_T):

$$C_T = 1 - \sum_i F_T(|\phi_i\rangle) = 1 - \sum_i |\langle T \otimes i | \phi_i \rangle|^2.$$





State Prep for GHZ State with One Ancilla

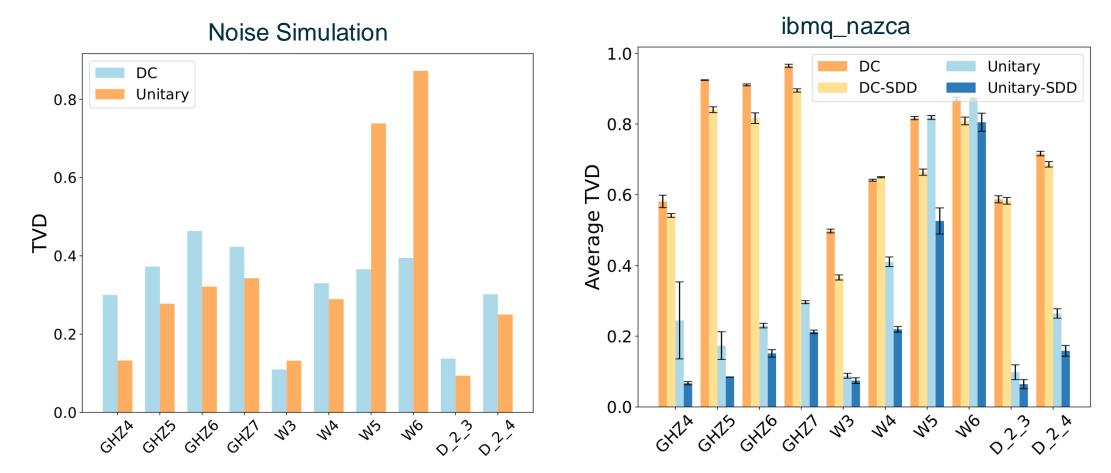


Dynamic circuits achieve shorter circuit depth

States	n	СМОТ		Depth	
		Unitary	Dynamic	Unitary	Dynamic
GHZ4	4	3	4	3	2
GHZ6	6	5	7	4	3
GHZ8	8	7	13	5	4

More ancillas in dynamic circuits can further reduce the circuit depth.

State Prep Validation on IBM Quantum Hardware

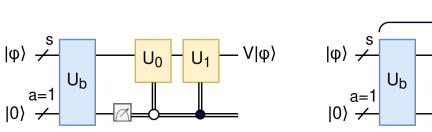


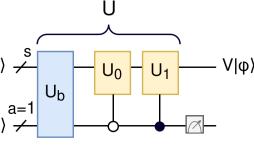
Noisy simulation results show that dynamic circuits sometimes obtain better fidelity (W states).

Unitary circuit - Hilbert Schmidt distance:

$$1 - \frac{1}{2^n} \left| \operatorname{Tr} \left(V^{\dagger} U \right) \right|$$

Unitary circuit - Hilbert Schmidt distance:

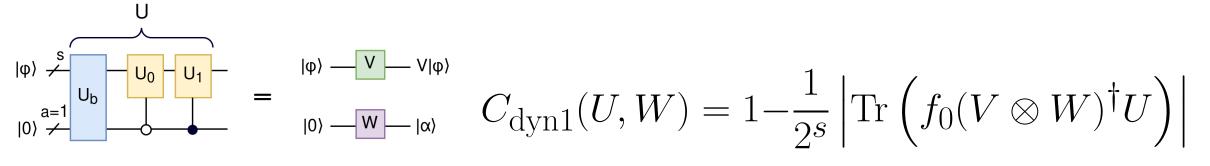




(b)

$$1 - \frac{1}{2^n} \left| \operatorname{Tr} \left(V^{\dagger} U \right) \right|$$

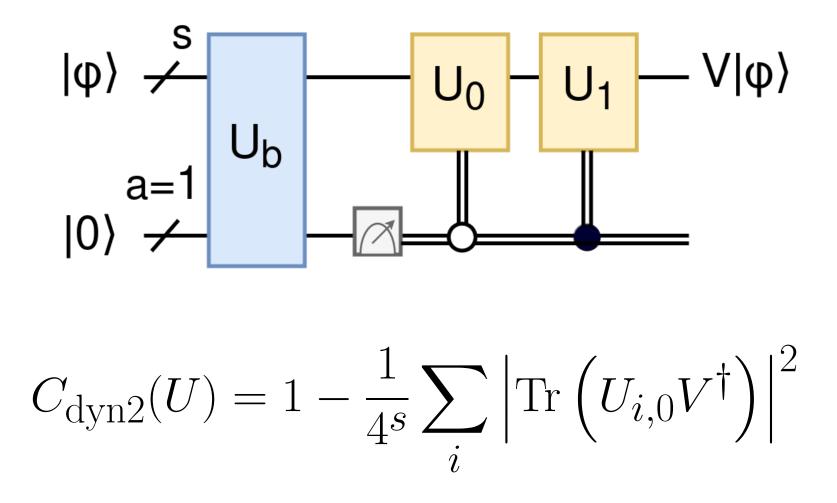
$$f_0 = I \otimes I \otimes \ldots I \otimes |0\rangle \langle 0|$$



(C)

(a)

First method for unitary preparation



Ancilla System $U = |0\rangle \langle 0| \otimes U_{00}$ $+|0\rangle \langle 1| \otimes U_{01}$ $+|0\rangle \langle 0| \otimes U_{10}$ $+|1\rangle \langle 1| \otimes U_{11}$ $= \begin{pmatrix} U_{00} & U_{01} \\ U_{10} & U_{11} \end{pmatrix}$

> The ordering of ancilla and system qubits determines elements

$$C_{\rm dyn1}(U,W) = 1 - \frac{1}{2^s} \left| \operatorname{Tr} \left(f_0 (V \otimes W)^{\dagger} U \right) \right|$$

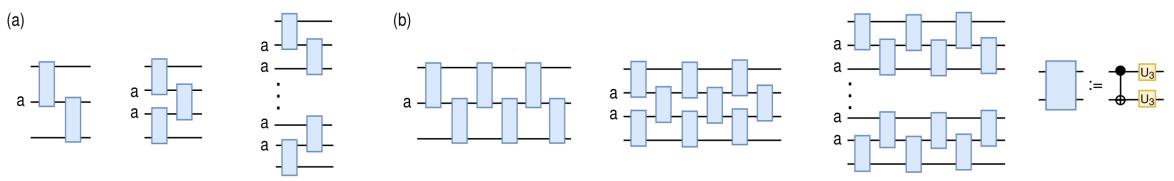
More parameters to optimize but less matrix multiplication

$$C_{\text{dyn2}}(U) = 1 - \frac{1}{4^s} \sum_{i} \left| \text{Tr} \left(U_{i,0} V^{\dagger} \right) \right|^2$$

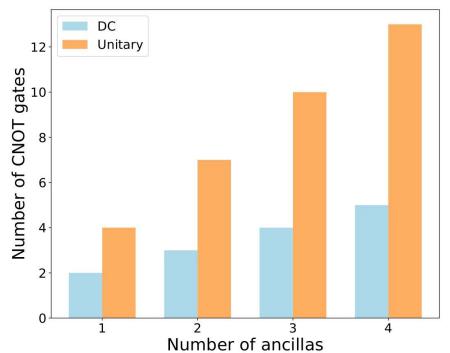
Less parameters to optimize but more matrix multiplication

Based on empirical experimental results **C**_{dyn1} is preferred

Dynamic Unitary Instantiation - Long Range Gates

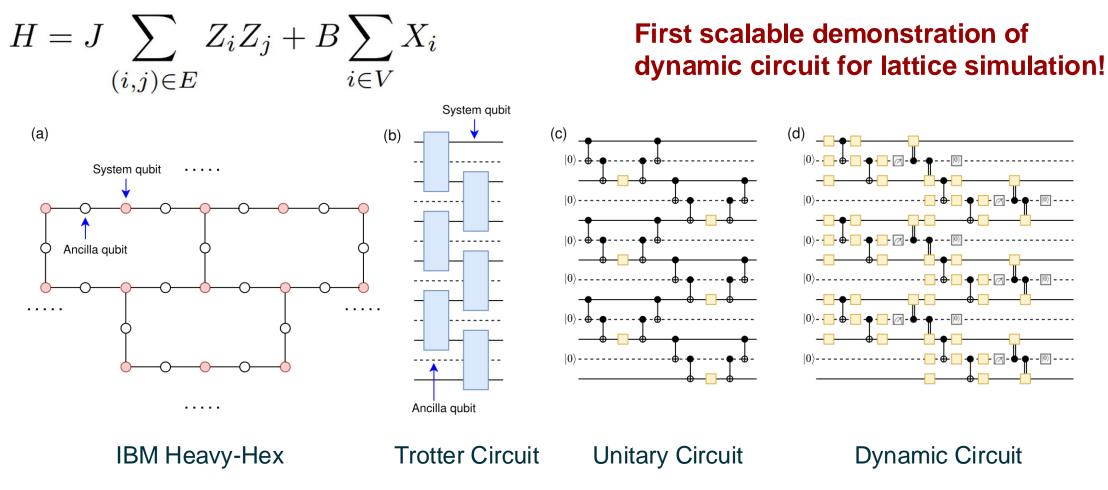


- Dynamic circuit
 - (a) Long-range CNOT/CZ/CS/Rzz/Rxx/Ryy
 - Depth: constant 2 O(1)
 - CNOT: n 1 O(n)
 - (b) Long-range generic two-qubit gate
 - Depth: constant 6 O(1)
 - CNOT: (n-1) x 3 O(n)
- Unitary circuits
 - circuit depth O(n)
 - CNOT: <u>O(n)</u>

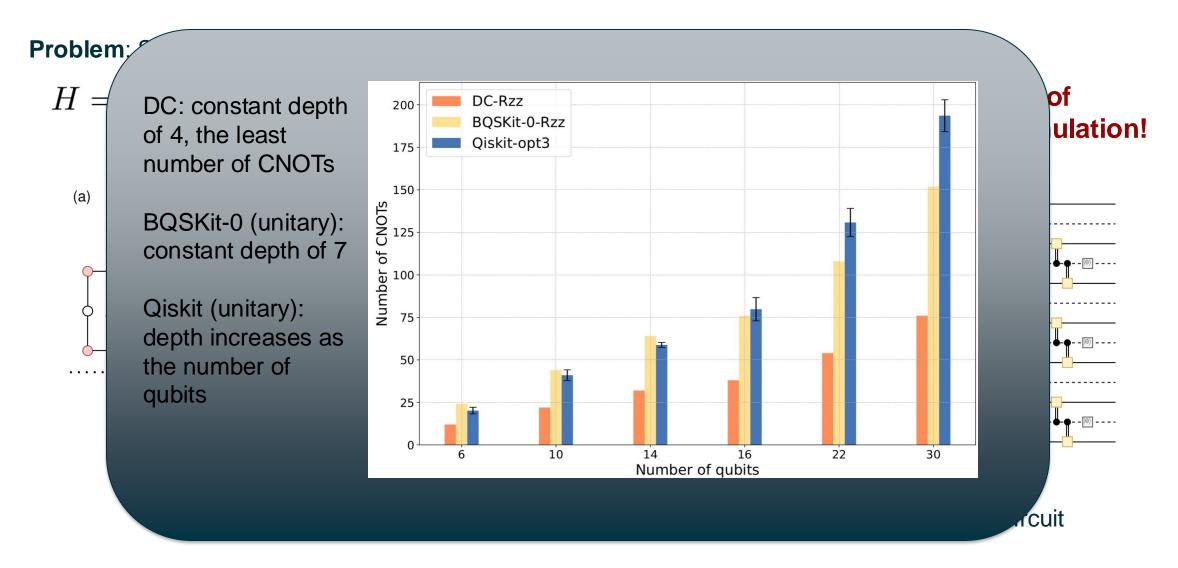


Dynamic Circuit Compilation for Lattice Simulation

Problem: Simulate time evolution of TFIM on a hexagonal lattice

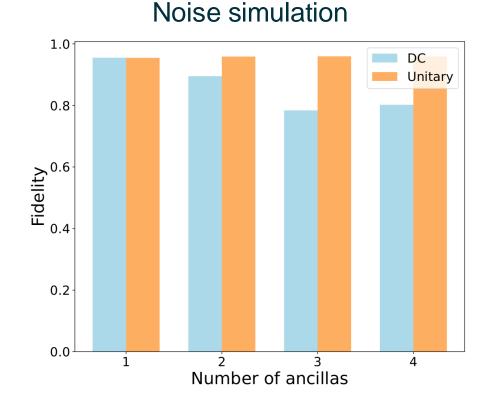


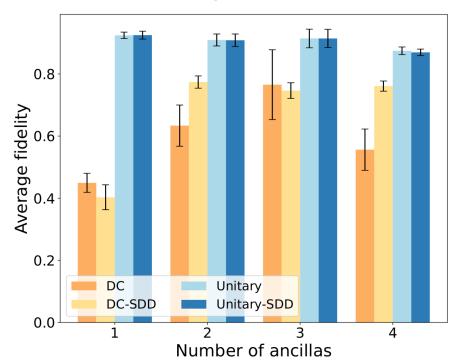
Dynamic Circuit Compilation for Lattice Simulation



Quantum Hardware Results - Long Range Gates

- Hardware characteristics
 - Measurement error: ~10x more than 2-q gate error, ~20x longer than 2-q gate duration
 - $_{\odot}$ Feed-forward loop: ~10x as long as 2-q gate duration
- Unitary circuits obtain higher fidelity due to the large error in mid-circuit measurement.



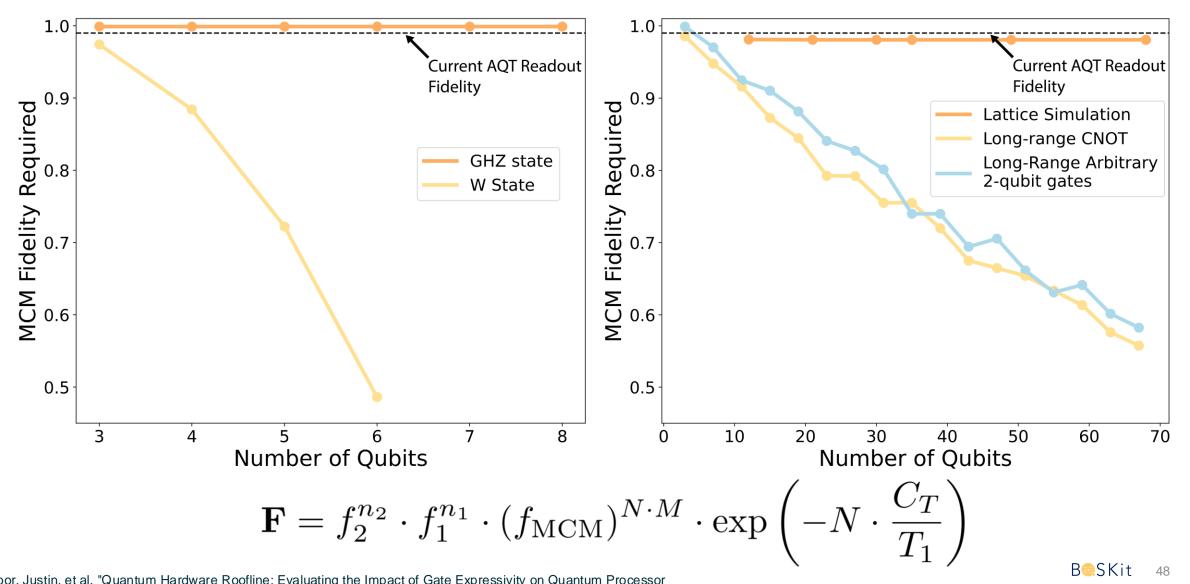


BOSKit

47

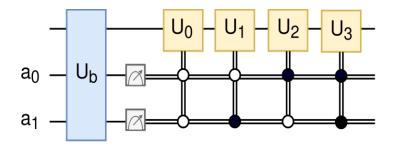
ibmq_nazca

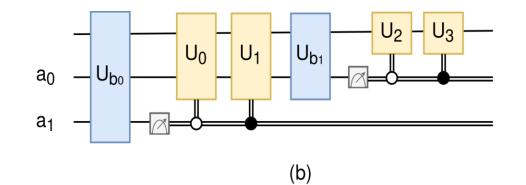
MCM Fidelity Projection Analysis



Kalloor, Justin, et al. "Quantum Hardware Roofline: Evaluating the Impact of Gate Expressivity on Quantum Processor Design." 2024 IEEE International Conference on Quantum Computing and Engineering (QCE). Vol. 1. IEEE, 2024.

Customizable Circuit Structure and Ancilla Count





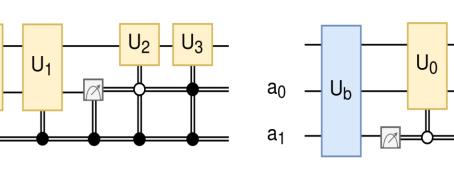


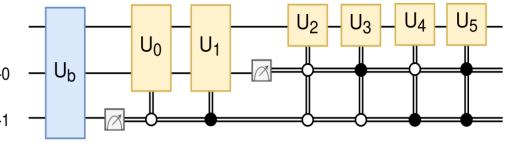
 U_0

 $a_0 = U_b$

a₁ -







(d)

(a) Simultaneous measurement (c) Asymmetric Nested measurement

(c)

(b) Independent measurement (d) Symmetric Nested measurement

Conclusions and Future Work

- Introduced BQSKit and the ongoing dynamic circuit work in the framework
- Next steps are to accelerate the math and release a major software update to BQSKit
- Upgrade the search step of synthesis to work on branched circuits
- Upgrade the partitioning methods in BQSKit to handle ancillas





bqskit.lbl.gov

Thank You!

from bqskit import Circuit, compile
circuit = Circuit.from_file('in.qasm')
out_circuit = compile(circuit)
out_circuit.save('out.qasm')

BQSKit is a powerful and portable quantum compiler framework

Tutorial and documentation online

Acknowledgements: DOE ASCR, ARQC, NERSC

We're always happy to collaborate

BCSKit



bqskit.lbl.gov